IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Docket No.: P27312

David S. COLLINS et al.

Serial No: 10/605,960 Group Art Unit: 2825

Confirmation No. 2959

Filed: November 10, 2003 Examiner: Paul Dinh

For: **ESD DESIGN, VERIFICATION AND CHECKING SYSTEM AND METHOD OF USE**

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Window, Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria, VA 22314

AMENDMENT UNDER 37 C.F.R. § 1.111

Sir:

In response to the **non-final Office Action** mailed **January 11, 2006** ("Office Action"), Applicant respectfully requests reconsideration of the application in view of the following Amendments and Remarks.

If extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned for under 37 C.F.R. § 1.136(a). Applicants believe that no further fees for net addition of claims are required at this time. Any fees required for further extensions of time and any fees for the net addition of claims are hereby authorized to be charged to **IBM Deposit Account No. 09-0456** (Burlington).

Amendments to the claims begin on page 2; and

Remarks begin on page 9.

AMENDMENT TO THE CLAIMS

In the Claims:

Please **CANCEL** claims 22-31;

Please **AMEND** claims 1, 3 and 19; and

Please **ADD** new claims 32-41.

A copy of all pending claims and a status of the claims is provided below.

1. (Currently Amended) A computerized ESD circuit design system, comprising:

a user interface for inputting a plurality of design parameters of a circuit;

an ESD kit comprising parameterized cells (p-cells) of low level electronic circuit components and p-cells of higher level electronic circuit components, the higher level electronic circuit components comprising growable and non-growable segments; and

a circuit schematic module creating ESD elements for connection with the circuit based on the plurality of design parameters and using at least one of the low level electronic circuit components and the higher level electronic circuit components.

2. (Original) The computerized ESD circuit design system of claim 1, wherein the circuit schematic module places the ESD elements in the circuit.

3. (Currently Amended) The computerized ESD circuit design system of claim 1, wherein said low level electronic circuit components and higher level electronic circuit components are in a hierarchical format.

4. (Original) The computerized ESD circuit design system of claim 1, wherein the higher level electronic circuit components form repetition groups of an underlying p-cell

element to accommodate different inputted design parameters when forming the ESD elements.

5. (Original) The computerized ESD circuit design system of claim 1, wherein the p-cells of lower order electronic components fix some variables and pass some variables to the higher order p-cell electronic components through inheritance.

6. (Original) The computerized ESD circuit design system of claim 1, further comprising a translation module for translating schematic representations of the ESD elements to graphical representations of the ESD elements and translating the graphical representations of the ESD elements to the schematic representations of the ESD elements.

7. (Original) The computerized ESD circuit design system of claim 1, further comprising a library containing various types of the ESD elements.

8. (Original) The computerized ESD circuit design system of claim 7, further comprising a module for manipulating the ESD elements to conform with a design of the circuit.

9. (Original) The computerized ESD circuit design system of claim 7, further comprising a pointer to the various types of the ESD elements in the library.

10. (Original) The computerized ESD circuit design system of claim 7, wherein the various types of the ESD elements are preset or user designed.

11. (Original) The computerized ESD circuit design system of claim 1, wherein the circuit schematic module creates one of a symbol and a schematic of the ESD elements.

12. (Original) The computerized ESD circuit design system of claim 1, further comprising a graphical seed module for creating a graphical seed of at least the ESD elements and the circuit.

13. (Original) The computerized ESD circuit design system of claim 12, wherein the graphical seed module includes functions of at least one of:

(i) Stretch,

(ii) Conditional Inclusion,

(iii) Repetition,

(iv) Parameterized shapes,

(v) Repeat along shape,

(vi) Reference point,

(vii) Inherited Parameters,

(viii) Parameterized Layer,

(ix) Parameterized Label,

(x) Parameterized Property,

(xi) Parameters, and

(xii) Compile.

14. (Original) The computerized ESD circuit design system of claim 12, wherein the graphical seed module creates a graphical representation of the circuit and the designed ESD element for future fabrication.

15. (Original) The computerized ESD circuit design system of claim 1, wherein the circuit schematic module creates a boundary about the ESD elements containing circuit information and places the schematic within the circuit design.

16. (Original) The computerized ESD circuit design system of claim 1, further comprising a module for providing modification of ESD interconnect parameterized cells based on information of the higher level electronic circuit components.

17. (Original) The computerized ESD circuit design system of claim 16, wherein said circuit schematic module provides a static p-cell substantiation translator box used for comparison of the ESD interconnect parameterized cell and robustness of the ESD kit.

18. (Original) The computerized ESD circuit design system of claim 16, further comprising a component to identify and verify a connection of at least one of a circuit type, the ESD interconnect parameterized cell, ESD type and a pad.

19. (Currently Amended) The computerized ESD circuit design system of claim 1, further comprising:

a cell substantiation translator module for identifying which components [[is]] are part of the higher level electronic circuit ~~elements~~ components;

a module for eliminating and preserving all of the higher level electronic circuit ~~elements~~ components in the cell substantiation translator module; and

a module for re-generation of all graphical information from the cell substantiation translator module based on the preserved higher level electronic circuit ~~elements~~ components for graphically representing the circuit and ESD elements.

20. (Original) The computerized ESD circuit design system of claim 1, further comprising a component to establish an interconnection path of a pad level for an input pad and to verify an ESD interconnect at the pad level.

21. (Original) The computerized ESD circuit design system of claim 1, wherein a p-cell is established which prevents a metal level to go below a given ESD width where a minimum width is established by conversion of a metal shape into the p-cell where the metal has an algorithm with a minimum function where the width never goes below a given width defined by a minimum ESD requirement.

Claims 22-31 (Canceled).

32. (New) The computerized ESD circuit design system of claim 1, wherein the low level electronic circuit components comprise growable and non-growable segments.

33. (New) The computerized ESD circuit design system of claim 1, wherein the circuit schematic module creating ESD elements for connection with the circuit based on the plurality of design parameters uses each of the low level electronic circuit components and the higher level electronic circuit components.

34. (New) The computerized ESD circuit design system of claim 1, wherein the system auto-wires ESD elements to create the circuit.

35. (New) The computerized ESD circuit design system of claim 1, wherein the system generates a schematic/symbol representation of the circuit and simulates the ESD elements that are placed and wired.

36. (New) The computerized ESD circuit design system of claim 1, wherein one of the p-cells is an ESD interconnect that provides ESD robustness.

37. (New) The computerized ESD circuit design system of claim 36, wherein the ESD interconnect is a hierarchical p-cell.

38. (New) The computerized ESD circuit design system of claim 36, wherein the ESD interconnect comprises a metal film.

39. (New) The computerized ESD circuit design system of claim 1, wherein the ESD elements are one of; resistor p-cells; transistor p-cells; and varactor p-cells.

40. (New) A computerized ESD circuit design system, comprising:

a user interface for inputting a plurality of design parameters of a circuit;

an ESD kit comprising parameterized cells (p-cells) of low level electronic circuit components and p-cells of higher level electronic circuit components, the higher level electronic circuit components comprising growable and non-growable segments; and

a circuit schematic module creating ESD elements for connection with the circuit based on the plurality of design parameters and using each of the low level electronic circuit components and the higher level electronic circuit components.

41. (New) A computerized ESD circuit design system, comprising:

a user interface for inputting a plurality of design parameters of a circuit;

an ESD kit comprising parameterized cells (p-cells) of low level electronic circuit components and p-cells of higher level electronic circuit components, the lower and higher level electronic circuit components comprising growable and non-growable segments; and

a circuit schematic module creating ESD elements for connection with the circuit based on the plurality of design parameters and using each of the low level electronic circuit components and the higher level electronic circuit components.

REMARKS

By this amendment, claims 1, 3 and 19 are amended, claims 22-31 are canceled, and claims 32-41 are added for the Examiner's consideration. The above amendments do not add new matter to the application and are fully supported by the specification. For example, support for new claims 32-41 can be found in original claim 1 and on paragraphs [0102], [0107], [0108] - [0113], [0125] and [0146] of the instant published application No. 2005/0102644. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

Allowed Claims

Applicants appreciate the indication that claim 19 contains allowable subject matter and would be allowed if presented in independent form. However, at this time, claim 19 has not been presented in independent form because it is believed that claim 1 is allowable. Moreover, Applicants submit that all claims are in condition for allowance for the following reasons.

Claim Objection

Claim 19 was objected to because it allegedly recites a feature lacking proper antecedent basis. This rejection is believed to be moot.

By this Amendment, Applicants have amended claim 19 in an effort to resolve this basis of objection.

Accordingly, Applicants respectfully request that the objection of claim 19 be withdrawn.

35 U.S.C. §112 Rejection

Claims 1-21 were rejected under 35 U.S.C. §112, 1st paragraph. This rejection is believed to be improper.

The Examiner asserts that the language "non-growable segments" in claim 1 lacks enabling support in the originally filed specification. Applicants respectfully disagree.

Paragraph [0102] of the instant published application No. 2005/0102644 specifically explains that "various parameters of the high level ESD circuit itself are fixed (i.e., non-growable) while others of the parameters are "grow-able" depending on the parameters and conditions specified by the user." Such language coupled with the knowledge of one having ordinary skill in the art provide full and clear enablement for the language recited in claim 1.

Accordingly, Applicants respectfully request that the rejection of claims 1-21 be withdrawn.

35 U.S.C. §102(b) Rejection

Claims 1-18, 20 and 21 are rejected under 35 U.S.C. §102(b) as being anticipated by publication entitled "A Design System for Auto-generation of ESD Circuits" by Steven H. Voldman et al. ("VOLDMAN"). This rejection is respectfully traversed.

In order to establish a *prima facie* case of anticipation under 35 U.S.C. § 102, a single prior art reference must disclose each and every element as set forth in the subject claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2

USPQ 2d 1051, 1053 (Fed. Cir. 1987). Applicants respectfully submit that a *prima facie* case of anticipation cannot be established because VOLDMAN fails to teach each and every element of the claims.

In particular, independent claim 1 recites, *inter alia,*

> an ESD kit comprising parameterized cells (p-cells) of low level electronic circuit components and p-cells of higher level electronic circuit components, the higher level electronic circuit components comprising growable and non-growable segments; and
> a circuit schematic module creating ESD elements for connection with the circuit based on the plurality of design parameters and using at least one of the low level electronic circuit components and the higher level electronic circuit components.

Applicants submit that VOLDMAN does not disclose, or even suggest, at least these features.

Applicants acknowledge, for example, that VOLDMAN discloses an ESD design cad system which uses p-cells "which are constructed into higher level ESD networks" (see first left-hand column on page 2, lines 3-4). The system also provides that "[l]owest order p-cells are RF and dc characterized" (see first left-hand column on page 2, lines 4-5). Additionally, the system also provides that "[t]he p-cells are grow-able elements which fix some variables, and pass some variables to the higher order circuit through "inheritance" (see first left-hand column on page 2, lines 12-15). However, the Examiner has not identified any language in VOLDMAN which discloses or suggests an ESD kit comprising parameterized cells (p-cells) of low level electronic circuit components and p-cells of higher level electronic circuit components, the higher level electronic circuit components comprising growable and non-growable segments and a circuit schematic module creating ESD elements for connection with the circuit based on the plurality of design parameters and using at least one of the low level electronic

circuit components and the higher level electronic circuit components.

Applicants emphasize that whereas the system in VOLDMAN apparently uses p-cells that are grow-able elements which fix some variables, and pass some variables to the higher order circuit through "inheritance", such language does not disclose or suggest the higher level electronic circuit components comprising growable and non-growable segments, and does not disclose or suggest using at least one of the low level electronic circuit components and the higher level electronic circuit components in a circuit schematic module.

Thus, Applicants respectfully submit that independent claim 1, and dependent claims 2-18, 20 and 21 are allowable.

Accordingly, Applicants respectfully submit that the rejection under 35 U.S.C. § 102(b) should be withdrawn.

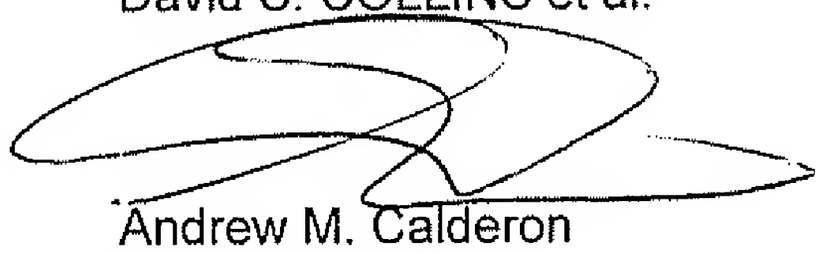
New Claims are also Allowable

Applicants submit that the new claims 32-41 are allowable over the applied art of record. Specifically, claims 32-39 depend from claim 1 which is believed to be allowable. For example, VOLDMAN does not disclose that the ESD element or p-cell can be an ESD interconnect or a wiring interconnect. Furthermore, claims 40 and 41 recite a combination of features which are clearly not disclosed or suggested by the applied art of record. Accordingly, Applicants respectfully request consideration of these claims and further requests that the above-noted claims be indicated as being allowable.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to **IBM Deposit Account No. 09-0456** (Burlington).

Respectfully submitted,
David S. COLLINS et al.



Andrew M. Calderon
Reg. No. 38,093

April 10, 2006
Greenblum & Bernstein, P.L.C.
1950 Roland Clarke Place
Reston, Virginia 20191
Telephone: 703-716-1191
Facsimile: 703-716-1180